ABSTRACT

A computer. An instruction pipeline and memory access unit execute instructions in a logical address space of a memory of the computer. An address translation circuit translates address references generated by the program from the program's logical address space to the computer's physical address space. Profile circuitry is cooperatively interconnected with the instruction pipeline and configured to detect, without compiler assistance for execution profiling, occurrence of profilable events occurring in the instruction pipeline, and is cooperatively interconnected with the memory access unit to record profile information describing physical memory addresses referenced during an execution interval of the program.